6 TO 18 GHz SINGLE-ENDED AND PUSH-PULL MMIC AMPLIFIERS FOR HIGH-GAIN MODULES

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ABSTRACT

Broadband single-ended and push-pull MMIC amplifiers are presented which achieve high gain per mA and demonstrate excellent cascadability. The single-ended 6 to 18 GHz amplifier shows 10 $\pm$1 dB gain for 25 mA current, which is the highest gain per mA reported for an amplifier in this band. The push-pull amplifier shows 10 dB gain for 50 mA current with a higher output power of 12 dBm at 1 dB gain compression, P(-1 dB). It also has the added features of gain equalization and gain control. A module designed with four push-pull chips shows excellent gain flatness of 34 $\pm$1 dB. Both of these MMICs are very compact (only 36 x 48 and 48 x 48 mils) and demonstrate high overall yield (>80%) due to the absence of via holes and other yield limiting process steps.

INTRODUCTION

Many military systems require high-gain (more than 30 dB) amplifiers in the 6 to 18 GHz band. MMIC amplifiers are ideal for these systems since they can reduce system costs in high volume while reducing size and increasing reliability. In recent years several good papers have been published on MMIC amplifiers covering the 6 to 18 GHz band [1,2,3,4,5]. Many system requirements are being met with existing MMICs, yet further improvements are required in the areas of power dissipation and efficiency, gain flatness at high gain levels, and chip yields and costs. MMIC amplifiers typically require 250-500 mA of current to achieve 40 dB of gain in the 6 to 18 GHz band. We present in this paper a unique set of MMIC chips which reduce DC current by a factor of 2 to 4 and still meet the system gain flatness and other requirements.

The single-ended amplifier presented here is designed for the highest gain efficiency (gain per mA). The push-pull amplifier is designed for higher output power, gain flatness, and cascadability for high-gain modules (more than 30 dB). Very high gain amplifiers have gain flatness and stability problems due to feedback and parasitic coupling. Since a push-pull amplifier maintains a virtual ground on the chip there is very little parasitic source inductance feedback. We have verified this experimentally by observing that the push-pull modules have better gain flatness at higher gain levels (greater than 30 dB) than the single-ended chips. Both MMIC chips use a standard ion-implanted production process with an F_t between 14 and 18 GHz at a bias of 0.5 I_{dss}.

SINGLE-ENDED AMPLIFIER DESIGN

Figure 1 shows a photograph of the single-ended amplifier. It is a three-stage amplifier with each stage using a 250 micron FET. Figure 2 shows the FET model with parameter values that were used in simulating the amplifier performance. Lossy matching networks are used in all three stages in order to obtain flat gain over the 6 to 18 GHz band. This also reduces the sensitivity of the amplifier response to process variations. The output stage uses drain to gate feedback to obtain good output match. Lumped elements are used throughout for the matching networks. This results in a very compact chip

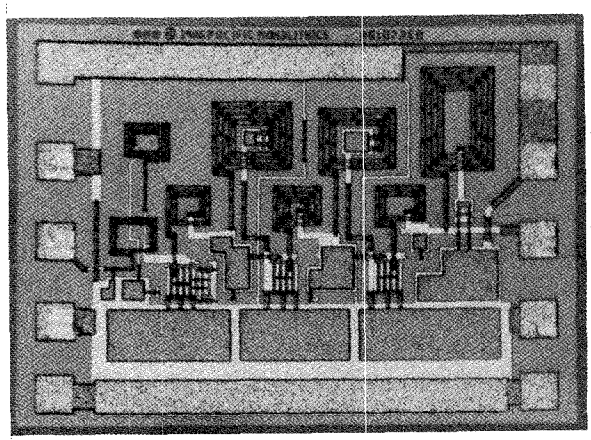

Figure 1. Photograph of Single-Ended 6 to 18 GHz MMIC Amplifier.

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(only 36 x 48 mils) for the single-ended design. The spiral inductors used in the matching networks are designed using a proprietary computer program that calculates the element values and the parasitics for a given layout. This program takes into account coupling between several adjacent conductors, ground plane effects, skin depth, etc. for high accuracy. The spiral inductor model has been verified experimentally up to 18 GHz. The capacitors are of MIM design and achieve 275 pF/sq. mm. Low valued resistors utilize an N^+ implant with low sheet resistance while the high-value resistors make use of the N^- implant which has a higher sheet resistance.

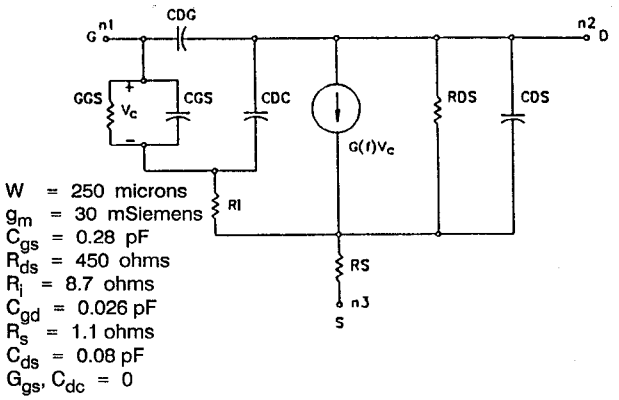

Figure 2. FET Model Used in RF Amplifier Simulation.

The DC biasing scheme for the amplifier consists of a novel totem-pole design that results in very low current consumption (only 25 mA). All three FETs are biased at approximately two-thirds I_{dss} in order to achieve maximum gain efficiency. The self-biased design eliminates the need for a negative gate voltage and results in single-supply operation. The source bypass capacitors are included on chip.

SINGLE-ENDED AMPLIFIER PERFORMANCE

The MMICs were characterized at the wafer level using Cascade Microtech RF probes. The coplanar nature of the probes makes it possible to achieve low-inductance grounds. Figure 3 shows the wafer-level gain and return loss measured on the new MMICs. The amplifiers typically exhibit 10 $\pm$1 dB gain across the 6 to 18 GHz band and draw 25 mA at a 9 Volt bias. The MMIC achieves a gain-to-current efficiency of 0.40 dB per mA. The maximum VSWR at the input and the output is 2.5:1. Figure 4 shows the performance of 26 of these MMICs measured across the wafer. They exhibit excellent uniformity and high net yield (85 %). Such a high RF yield and repeatability could be achieved because of small chip size (made possible by the use of lumped element matching networks) and a simple ion-implanted process without via holes.

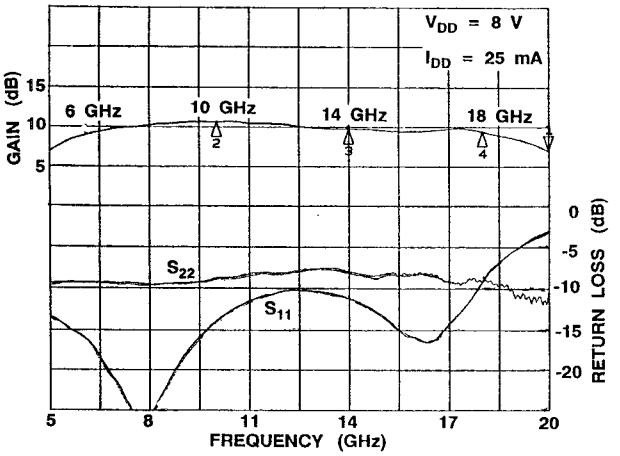

Figure 3. Wafer Level Performance of Single-Ended MMIC Amplifier.

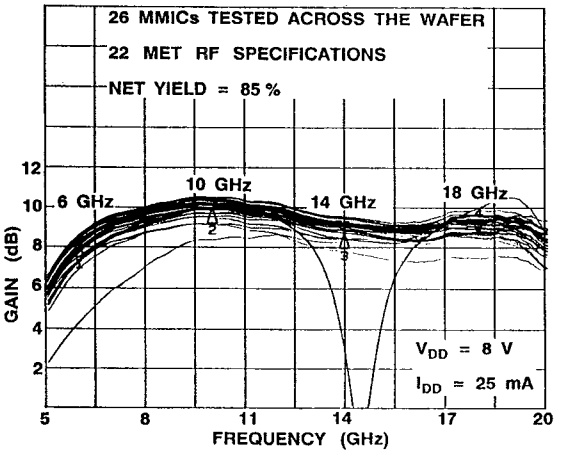

Figure 4. Wafer Level Performance of 26 MMICs Measured Across the Wafer.

Figure 5 shows the gain of a typical MMIC mounted on a carrier with 50 ohm lines. The minimum grounding inductance was achieved using several bond wires. The assembled amplifier demonstrates 9 $\pm$1 dB gain over the 6 to 18 GHz band. This includes losses in the connectors and the 50 ohm lines. The peaking in the gain response at the high end of the band is caused by the ground inductance of the bond wires. The effects of this lead inductance and parasitic feedback are further magnified in cascaded gain modules. A two-stage amplifier built using these MMICs exhibits 18 $\pm$2 dB gain over the 6 to 18 GHz band. It will be shown that for high-gain modules the push-pull amplifier demonstrates superior cascadability.

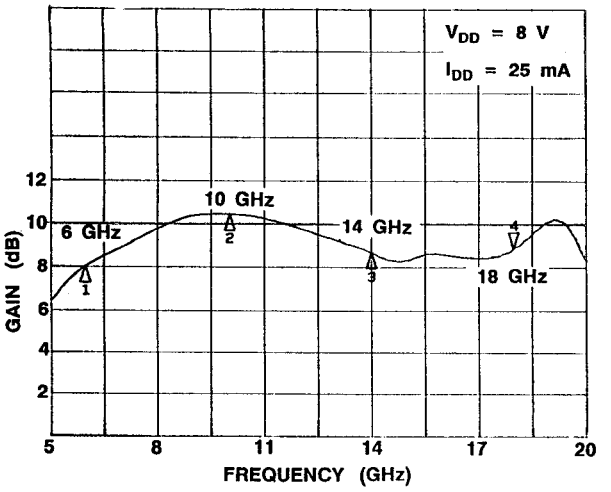

Figure 5. Gain of Single-Ended MMIC Mounted on a Carrier.

The noise figure of the MMIC amplifier (including fixture losses) was measured to be under 8 dB from 10 to 18 GHz with a peak value of 10 dB at 6 GHz. The MMIC also demonstrates a 1 dB gain compression point, P(-1 dB), of greater than 12 dBm in the 10 to 18 GHz range which drops to 8.5 dBm at 6 GHz. The reduced performance at the low end of the band both in noise figure and P(-1 dB) is attributed to the use of lossy matching networks with resistive characteristics at low frequencies.

PUSH-PULL AMPLIFIER DESIGN

Source inductance adversely affects the gain flatness of a single-ended amplifier and this effect is magnified and difficult to compensate for in broadband designs. High-frequency amplifiers minimize the source inductance by using via holes or wrap-around grounds. These are relatively complex process techniques that reduce the yield considerably. An alternative approach to achieve effective low source inductance is the use of the push-pull configuration. In this technique two single-ended amplifiers with their grounds tied together are driven 180 degrees out of phase using a balun. This creates a virtual ground within the chip between the two amplifiers and eliminates the need for physical grounding of the common node. It also eliminates the need for source bypass capacitors, thus reducing chip size.

Figure 6 is a photograph of the push-pull 6 to 18 GHz amplifier chip (48 x 48 mils). It consists of two identical single-ended amplifiers with their ground nodes connected. The design of this amplifier is very similar to that of the single-ended amplifiers. This circuit also contains a gain equalization scheme that uses an FET as a variable resistor to control the gain at the low end of the band. An external control voltage can be applied to shape the low-end gain response to compensate for process variations and achieve the desired gain flatness.

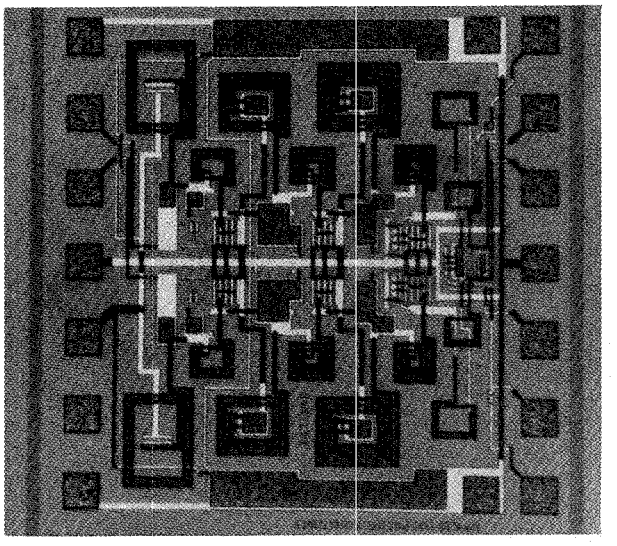

Figure 6. Photograph of Push-Pull 6 to 18 GHz MMIC Amplifier.

PUSH-PULL AMPLIFIER PERFORMANCE

Figure 7 shows the measured wafer level performance of this chip. The gain is 10 $\pm$0.75 dB over the 6 to 18 GHz band. The usable bandwidth extends from 5 to 20 GHz. The gain over a major portion of the band is flat to within $\pm$0.5 dB. This gain flatness without any tuning was possible because of the very low effective source inductance inherent in a push-pull circuit. The

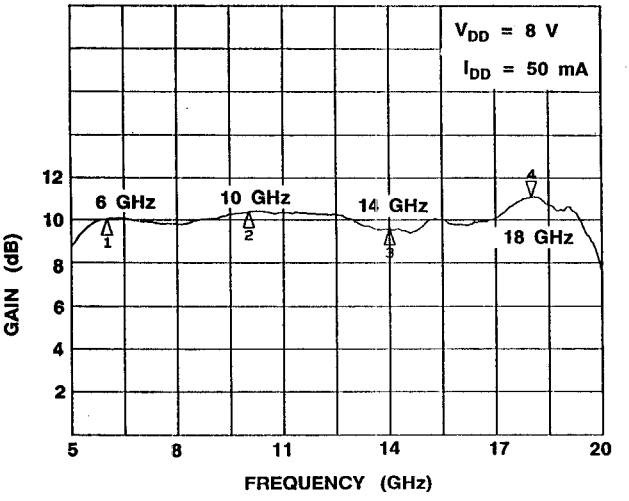

Figure 7. Wafer Level Performance of Push-Pull MMIC Amplifier.

small increase in gain at the high end of the band was designed in to compensate for higher losses in external circuitry. The maximum VSWR at the input and the output is 2.5:1. Figure 8 is a photograph of a four-stage amplifier module that was built using this chip for a 7 to 17 GHz system application. It consists of four push-pull amplifier MMICs cascaded between two coplanar type MIC baluns.

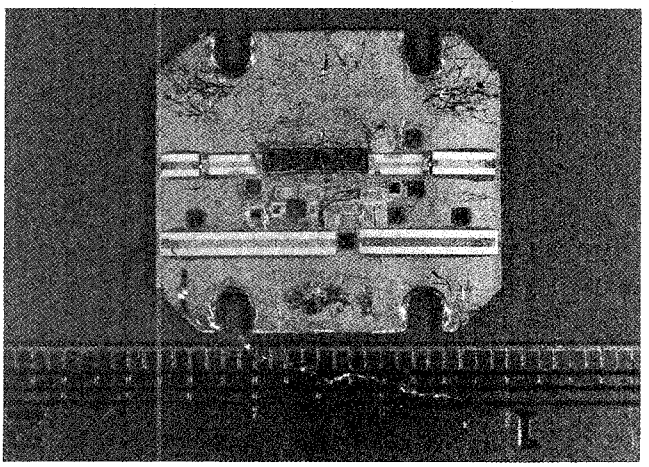

Figure 8. Photograph of Four-Chip High-Gain Amplifier Module.

The entire amplifier assembly fits within a carrier 600 mils wide. Figure 9 shows the results measured on this module. The gain of 34 $\pm$1 dB was achieved without any tuning. The presence of a virtual ground within the chip suppresses parasitic feedback between the amplifiers and contributes to stability and gain flatness even at high gain levels. Figure 10 shows the measured results on a two-stage amplifier module. It has a gain of 16 $\pm$1 dB over the 6 to 18 GHz band.

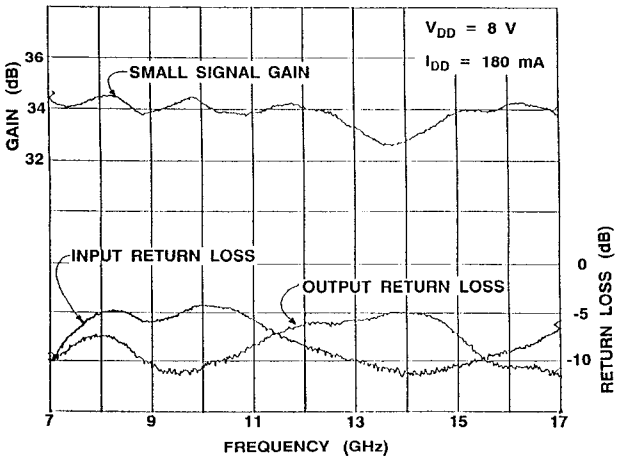

Figure 9. Performance of Four-Chip (Push-Pull) High-Gain Amplifier Module.

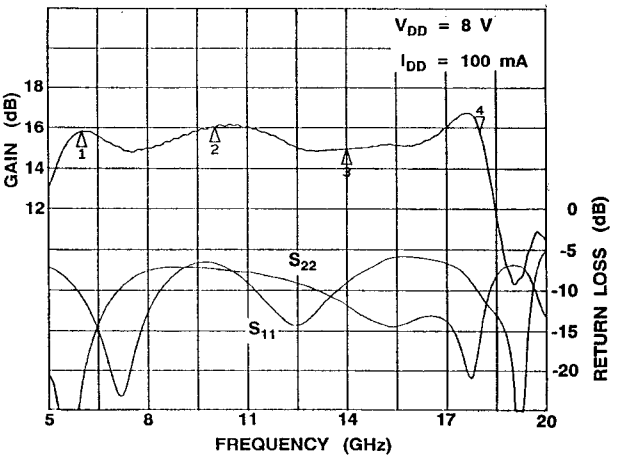

Figure 10. Performance of Two-Chip Amplifier Module.

CONCLUSION

A 6 to 18 GHz single-ended MMIC amplifier has been developed that demonstrates very high gain per mA of current. A push-pull amplifier technique has also been demonstrated beyond 18 GHz which eliminates the need for via holes and produces easily cascadable, high-yield MMICs. A 34 dB gain amplifier has been built utilizing this MMIC which achieves $\pm$1 dB flatness.

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